Abstract of the Disclosure

A pipelined multistreaming processor has an instruction source, a first cluster of a plurality of streams fetching instructions from the instruction source, a second cluster of a plurality of streams fetching instructions from the instruction source, dedicated instruction queues for individual streams in each cluster, a first dedicated dispatch stage in the first cluster for dispatching instructions to execution units, and a second dedicated dispatch stage in the second cluster for selecting and dispatching instructions to execution units. The processor is characterized in that the clusters operate independently, with the dedicated dispatch stage taking instructions only from the instruction queues in the individual clusters to which the dispatch stages are dedicated. In preferred embodiments there are dedicated fetch and dispatch stages for streams in the clusters, and dedicated execution units to which instructions may be dispatched.